

Patrick Craig

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Education

University of Florida

Gainesville, FL

Doctor of Philosophy, Electrical and Computer Engineering GPA: 3.62, Expected Graduation: May 2027
Relevant Coursework: Stochastic Methods I, Foundations of Digital Signal Processing, Signals and Systems, Estimation and Decision Theory, Fundamentals of Machine Learning

University of Florida

Gainesville, FL

Bachelor of Science, Electrical Engineering May 2023
Relevant Coursework: Applied Machine Learning, Foundations of Digital Signal Processing, Communication Systems

Skills

- **Programming & Test Automation:** Python, C++, MATLAB
- **Data Analysis & Characterization:** NumPy, Pandas, SciPy, Matplotlib
- **Semiconductor Test & Validation:** Device characterization, failure analysis, Klayout
- **Laboratory Instrumentation:** Oscilloscopes, DC power supplies, multimeters
- **Non-Destructive Evaluation:** Optical microscopy, X-ray CT/Laminography, Scanning Acoustic Microscopy (SAM)
- **Hardware-Software Integration:** Measurement data acquisition, test result analysis

Experience

Security and Assurance Laboratory

Gainesville, FL

Graduate Research Assistant

May 2023 – Current

- Doctoral researcher with **5+ years of experience** in semiconductor characterization, advanced packaging inspection, failure analysis, and multimodal metrology workflows for heterogeneous integration systems
- Served as technical lead for a **\$1M+ NSF Engines-funded semiconductor R&D initiative**, leading development of **multimodal datasets** for advanced packaging inspection, AI-assisted failure analysis, and semiconductor metrology workflows
- Developed multimodal semiconductor characterization workflows integrating optical microscopy, **X-ray CT/laminography** (Sigray Apex Hybrid), **scanning acoustic microscopy** (Nordson Sonoscan), and near-field **THz-TDS** (Protemics TeraCube), enabling analysis of defect mechanisms and process-induced variability
- Designed experimental inspection and validation workflows for heterogeneous integration structures, supporting **multiple federally funded and industry-sponsored semiconductor research programs**
- Investigated relationships between imaging physics, material properties, and defect observability across non-destructive characterization modalities, contributing to **15+ conference presentations, journal publications, and technical demonstrations**

Northrop Grumman

Colorado Springs, CO

Hardware and Logistics Intern

May 2022 – July 2022

- Performed system-level performance analysis of SATCOM and RADAR subsystems, evaluating communication efficiency, robustness, and architectural constraints
- Supported architectural **trade-off studies** by assessing algorithmic and system-level design choices impacting performance, reliability, and integration
- Authored and maintained **hardware and system documentation**, translating technical requirements into clear, verifiable specifications
- Developed and validated electrical system requirements aligned with performance metrics, interface definitions, and program-level specifications

Curated Projects and Publications

This is not a comprehensive list of publications or projects. Full list of publications here:

<https://scholar.google.com/citations?user=wmn2z3QAAAAJ&hl=en>

Research Collaboration: Multimodal X-ray Characterization of Through-Glass Via (TGV)

SCAN Laboratory / National Institute of Standards and Technology (NIST)

Summer 2026

- Collaborated with **NIST** on multimodal X-ray characterization studies of advanced through-glass via (TGV) and redistribution layer (RDL) structures for heterogeneous integration and advanced packaging applications
- Designed and executed experimental imaging workflows using **X-ray computed tomography (XCT)** and **X-ray laminography (XCL)** across multiple wafer-scale and die-scale samples with voxel resolutions ranging from **5 μm to 300 nm**
- Characterized high-aspect-ratio TGV structures with via pitches spanning **100–400 μm** , investigating void formation, Cu pullout behavior, delamination, interface defects, and process-induced variability across bonded and freestanding wafer configurations
- Developed region-of-interest (ROI) imaging and montage acquisition strategies to optimize throughput, defect detectability, and cross-sectional correlation across large-area semiconductor structures
- Supported comparative analysis between X-ray modalities to evaluate defect observability limitations and improve non-destructive semiconductor inspection methodologies

ISTFA2026: Multimodal Characterization Dataset Development for HBM3 Memory

Security and Assurance Laboratory, University of Florida

2025 – Current

- Developed a large-scale multimodal characterization dataset for **NVIDIA H100 HBM3 memory systems**, integrating **X-ray CT/laminography** and scanning acoustic microscopy for advanced packaging inspection and defect analysis
- Performed non-destructive imaging and analysis of HBM interconnects, microbumps, TSVs, substrate interfaces, and multilayer package structures
- Generated and curated **thousands of annotated defect and interconnect features** to support development of **agentic AI workflows** for semiconductor inspection, automated failure analysis, adaptive defect localization, and advanced packaging metrology research

Research Collaboration: Sandia National Laboratories LDRD Semiconductor Assurance Project

Security and Assurance Laboratory / Sandia

2025 – Current

- Contributed to a **\$130K Sandia National Laboratories LDRD-funded research initiative** focused on semiconductor assurance, advanced packaging security, and material-aware X-ray characterization workflows for microelectronics systems
- Developed multimodal inspection and visualization workflows integrating **multi-energy X-ray CT/laminography** and spectral reconstruction techniques to analyze material properties and defect behavior in electronic assemblies
- Investigated methods for reconstructing and visualizing **effective atomic number and electron density** within 3D X-ray volumes for material-aware semiconductor analysis and validation
- Developed software and data-processing pipelines for **material-aware 3D PCB and microelectronics reconstruction**, including GERBER-to-material representations, spectral CT integration, and layer-alignment visualization tools